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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,100	08/30/2006	Takahisa Tanabe	Q94049	9790

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EXAMINER	
CRAWLEY, KEITH L	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,100	TANABE, TAKAHISA	
	Examiner	Art Unit	
	KEITH CRAWLEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/31/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 8-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawasaki et al. (US 2004/0061671).

Regarding claim 1, Kawasaki discloses a display apparatus with an active matrix display panel having a plurality of pixel sections each including a light emitting element and a thin film transistor (fig. 2, see ¶ 73),

said display apparatus comprising: a power supply for supplying a supply voltage to said plurality of pixel sections (figs. 1 and 3, power supply inherent, see ¶ 73-74);

and display control means for sequentially specifying one of a plurality of rows of said display panel at a predetermined timing for each frame and at least one pixel section including a light emitting diode to be driven for light emission in the one row (fig. 3, scanning driver 301 and signal driver 303, see ¶ 75),

supplying a display scanning pulse to each pixel section in the one row (fig. 1, first Vg pulse, see ¶ 75),

supplying a data pulse indicative of a first gate voltage of said thin film transistor to the at least one pixel section when supplying the display scanning pulse (fig. 1, signal voltage Vs is applied to the gate of Tr2 during time period T1, see ¶ 75-76),

subsequently supplying a reset scanning pulse each of said pixel sections in the one row (fig. 1, second Vg pulse, see ¶ 77),

and supplying a reset pulse to the at least one pixel section when supplying the reset scanning pulse (fig. 1, threshold value control voltage Vr is applied to the gate or Tr2 during time period T2, see ¶ 77),

the reset pulse indicating a second gate voltage of said thin film transistor for making the polarity of a gate-to-source voltage or gate-to-drain voltage of said thin film transistor reverse to the polarity during light emission driving (see ¶ 76 and end of ¶ 77, see also ¶ 80),

wherein: each of said plurality of pixel sections has a driving unit for supplying a gate of said thin film transistor with the first gate voltage corresponding to the data pulse in response to the display scanning pulse (figs. 2 and 3, signal driver 303 applies Vs via signal lines to gate of Tr2, see ¶ 75-76),

and for supplying the gate of said thin film transistor with the second gate voltage corresponding to the reset pulse in response to the reset scanning pulse (figs. 2 and 3, signal driver 303 applies Vr via signal lines to gate of Tr2, see ¶ 77).

Regarding claim 2, Kawasaki discloses wherein an absolute value of the gate-to-source voltage or gate-to-drain voltage of said thin film transistor depending on the first gate voltage is equal to an absolute value of the gate-to-source voltage or gate-to-drain voltage of said thin film transistor depending on the second gate voltage (¶ 80-81, Vs is equal to absolute value of Vr).

Regarding claim 3, Kawasaki discloses wherein the gate-to-source voltage or gate-to-drain voltage of said thin film transistor depending on said second gate voltage is a fixed voltage (¶ 88, Vr may be set to a constant voltage).

Regarding claim 4, Kawasaki discloses wherein each frame period has a display mode period in which the gate of said thin film transistor is supplied with the first gate voltage (fig. 1, time period T1, see ¶ 73),

and a reset mode period in which the gate of said thin film transistor is supplied with the second gate voltage (fig. 1, time period T2, see ¶ 73).

Regarding claim 8, Kawasaki discloses wherein said light emitting element is an organic electroluminescence element (fig. 2, organic EL element 201).

Regarding claim 9, Kawasaki discloses wherein said thin film transistor is an amorphous silicon thin film transistor (¶ 83).

Regarding claim 10, Kawasaki discloses wherein said thin film transistor is an organic semiconductor thin film transistor (¶ 84).

Regarding claim 11, this claim is rejected under the same rationale as claim 1.

Regarding claim 12, this claim is rejected under the same rationale as claim 8.

Regarding claim 13, this claim is rejected under the same rationale as claim 9.

Regarding claim 14, this claim is rejected under the same rationale as claim 10.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki in view of Kubota et al. (US 5,748,165).

Regarding claim 5, Kawasaki discloses wherein a pixel section is in a display mode period in which the gate of said thin film transistor is supplied with the first gate voltage (fig. 1, time period T1, see ¶ 73)

and a reset mode period in which the gate of said thin film transistor is supplied with said second gate voltage (fig. 1, time period T2, see ¶ 73).

Kawasaki fails to disclose a pixel section which is supplied with the first gate voltage **in one frame period changes** to a reset mode period in which the gate of said thin film transistor is supplied with said second gate voltage **in the next frame period** [emphasis added].

Kubota teaches a pixel section which is supplied with the first gate voltage **in one frame period changes** to a reset mode period in which the gate of said thin film transistor is supplied with said second gate voltage **in the next frame period** [emphasis added] (figs. 16 and 17, see col. 20, line 43-col. 21, line 7, positive polarity data and negative polarity data are alternately written to the data lines on a field-by-field basis, thus a column supplied with the first gate voltage in one field is supplied with the second gate voltage in the next field, see also col. 31, line 53-58, driving system can be applied to active matrix EL display).

Kawasaki and Kubota are both directed to driving methods and systems for active matrix EL displays. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the display of Kawasaki with the driving system of Kubota since such a modification reduces power consumption, manufacturing cost, and operating cost (Kubota, abstract) and prevents degradation of the switching element (Kawasaki, ¶ 10).

Regarding claim 6, Kawasaki discloses wherein said pixel section comprises two equivalent driving circuits each have said thin film transistor (figs. 11 and 12, scanning circuit and threshold value control scanning circuit, see ¶ 100-101),

and said two driving circuits alternately switch the display mode and the reset mode (fig. 10, time periods T1 and T2, see ¶ 102-103).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki in view of Kimura (US 2003/0025656).

Regarding claim 7, Kawasaki fails to disclose wherein the display mode period and said reset mode period are repeated based on a sub-field method in each frame period.

Kimura teaches wherein the display mode period and said reset mode period are repeated based on a sub-field method in each frame period (fig. 4, display periods Tr1 and Tr2 and erasure periods Te1 and Te2, see ¶ 122 and ¶ 128-129).

Kawasaki and Kimura are both directed to driving methods and systems for active matrix EL displays. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the display of Kawasaki with the display of Kimura since such a modification achieves good display performance without an increase in power consumption (Kimura, ¶ 15) and prevents degradation of the switching element (Kawasaki, ¶ 10).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sung (US 6,677,713) discloses a light-emitting device display technique and a driving technique of an active matrix organic light-emitting diode (AMOLED) to increase the stability of threshold voltage as a function of time.

Miyazawa (US 7,345,685) discloses an electronic apparatus in which first and second switching transistors are turned on and an operation voltage Vdx and a data-current Idata are transmitted to a holding capacitor. Then, a first switch is turned off, a second switch and the second switching transistor are turned on, and a reset voltage Vr is transmitted to the holding capacitor, whereby the driving transistor is turned off and the organic EL element stops emitting light.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH CRAWLEY whose telephone number is (571)270-7616. The examiner can normally be reached on M-F, 7:30-5:00 EST, alternate Fri. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571)272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629

/KEITH CRAWLEY/
Examiner, Art Unit 2629